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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,792	HER ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *5,6 and 12-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-11,16 and 17* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are present for examination. Acknowledgment is made that claims 5 and 6 along with claims 12-15 have been canceled by applicant and may not be given further consideration within this examination of the instant application with regards to the remaining claims, claims 1-4, 7-11, and 16-17.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/17/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that no Information Disclosure Statement (IDS) was provided with the instant application.

Response to Arguments

Applicant's arguments with respect to claim 1-4 and 7-11 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features as described below must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings filed with this application are objected to since the figures do no illustrate the invention as it has been claimed by the applicant within the application. Specifically, the figures do not illustrate as claimed within claim 1 the providing a first group of output signals to a first group of output pins and a second group of output signals to a second group of output pins within respected test cycles, which indicates the two groups of output pins are different form one. The figures illustrate both a first and second group of output signals are provided to the same group of output pins supplying the signals to a device receiving the signals that has less pins.

Furthermore the figures do not illustrate as indicated within claim 3 wherein odd output signals are sent to odd output pins and even output signals are sent to even output pins in respective test cycles. Examiner notes that this format does not reduce

pins required by an external device receiving outputs from a device have more pins, rather it partitions the outputs supplied to the receiving device into two different cycles wherein all outputs are provided to their respective output pins but within a specific test cycle requiring any device receiving the output signals to have the same number of input pins as output pins of the device it is receiving the signals from to receive the signals. Examiner further notes that with respect to claim 4 similar not illustrated issues exists that are similar to those of claim 3, wherein the even/odd output signals are merely shifted to the odd/even output pins in a respective test cycle.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1-4, 11 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 indicates no reduced pin configuration as indicated by the applicant to be the intended claimed invention (see applicants arguments filed on 09/29/2006 and the applicants specification). The claim indicates that a first and second group of output signals are provided to a first and second group of output pins during respective test cycles within test mode, which indicates as described above within the objection to the figures that the two groups of output pins are different from one another. For purposes of this examination the second group of data output pins will be treated as being "the

group" or "the first group" of output pins as is understood by the examiner after review of the application.

Claims 3-4 indicate no reduced pin configuration as indicated by the applicant to be the intended claimed invention (see applicants arguments filed on 09/29/2006 and the applicants specification). As described above the claims do not produce a format in which any device receiving output signals from the device could have any amount of signal input pins less then the amount of signal output pins of the device it is receiving the signals from. For purposes of this examination the selection of output signals within the second test cycle will be treated as being supplied to the same set of output pins that are selected and provided output signals to within the first test cycle. Examiner suggests changing within claim 3 the second "even" to "the odd" and within claim 4 changing the second "odd" to "the even" to overcome the 112-second paragraph rejection.

Claims 2-4 are dependent upon claim 1 and therefore also inherit the 35 U.S.C. 112, second paragraph issues and as such may not be further considers on their merits.

Claim 11 indicates that an output is outputted twice from the semiconductor integrated circuit via two different output pins in two different phases which is not in accordance or is contradictory with respect to the claims that claim 11 is dependent upon. The claim indicates sending "(i+1)th" output signals to "ith" output data pins wherein "i" is a positive integer indicates a series of output signals is supplied to a series of output pins. However "ith" series of outputs was already been outputted to "ith" output data pins wherein "i" is a positive integer within the preceding claim (claim 9),

indicating that "(i+1)" output signal had already been outputted to "i+1" output data pin within the serial of "ith" output signals supplied to "ith" output data pins (direct pin to pin configuration). Furthermore it is claimed within the independent claim that the remaining output signals provided to the output pins within the second phase of the test mode are different from the output signals provided to the data output pins, thus sending "i+1" output signal to "i+1" output data pin within a first phase of the test mode and then sending "i+1" output signal to what would then be "i+2" output data pin would be contradictory to that claim within claim 9 in view of claim 7.

Claim 17 recites the limitation "i" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that claim 17 is dependent upon claim 7 wherein there is no "i" limitation introduced. Examiner further notes that the claim will be treated for purposes of this examination as being dependent upon claim 9 as claim 10 is wherein the limitation "i" is first introduced.

Appropriate correction and/or explanation is required to overcome the 35 U.S.C. 112, second paragraph rejections.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 7-8, and 16 are rejected under 35 U.S.C. 102(e) as being unpatentable over Deb et al (U.S. Patent 6971045 B1) filed May 20, 2002.

1. As per claims 1 and 7, Deb teaches a semiconductor integrated circuit/method comprising:

A plurality of data output pins (118h-p within figure 5 and column 11 line 54 – column 12 line 50);

A data processing circuit to generate output signals responsive to an input signal (104 in figure 1 and/or 104a or 122 in figure 5, column 2 line 11-15 and 35-43, and column 11 line 54 – column 12 line 56);

An output selection circuit with at least a normal mode and a test mode (124 in figures 1 and 4 with column 4 lines 38-52, or 142a-d, 144a-d, and 158a-d in figure 5 with column 12 lines 30-56);

Where a first group of output signals are provided to a first group of data output pins in a first test cycle of the test mode (see column 12 lines 1-50 and figure 5); and

Where a second group of output signals are provided to a second group of data output pins during a second test cycle of the test mode (see column 12 lines 1-50 and figure 5).

2. As per claims 2 and 8, Deb teaches the semiconductor integrated circuit/method where the output selection circuit repeats the first and second test cycles during testing (column 1 lines 18-21 with column 12 lines 1-3 and 51-56).

3. As per claim 16, Deb teaches the semiconductor integrated circuit where the output selection circuit is adapted to send all output signals to corresponding output pins during the normal mode (column 4 lines 38-42 and figures 1 and 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-4, 9-11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deb et al (U.S. Patent 6971045 B1).

4. As per claims 3, 9, 10, and 17, Deb teaches the circuit/method as described above with respect to claims 1 and 7.

Deb does not specifically teacher wherein the semiconductor integrated circuit/method where the output selection circuit sends odd output signal to odd data output pins during the first cycle of the test mode; and where the output selection circuit sends even output signal to even output pins during the second test cycle of the test mode.

However those of ordinary skill within the art at the time the invention was made would recognize that the output selection circuitry is not only limited to sending odd

output signals to odd data output pins during a first cycle of the test mode and sending even output signals to even output pins during a second cycle of the test mode. Those of ordinary skill in the art at the time the invention was made would recognize that any such configuration is well known when dealing with controllable switch-matrix output selection circuitry.

Therefore those of ordinary skill within the art at the time of the invention would have been motivated to have the output selection circuit configured to output such outputs within the different cycles of the test mode within Deb wherein a tester or circuitry/device/unit receiving the output signals is configured to identify the outputs in such a way, such that a proper result can be accredited to the proper corresponding test and subsequent tested circuitry.

5. As per claim 4, Deb teaches the circuit/method as described above.

Deb does not specifically teacher the semiconductor integrated circuit wherein the output selection circuit sends odd output signals to even data output pins during the first cycle of the test mode; and where the output selection circuit sends even output signals to odd output pins during the second test cycle of the test mode.

However those of ordinary skill within the art at the time the invention was made would recognize that the output selection circuitry is not only limited to sending odd output signals to even data output pins during a first cycle of the test mode and sending even output signals to odd output pins during a second cycle of the test mode. Those of ordinary skill in the art at the time the invention was made would recognize that any

such configuration is well known when dealing with controllable switch-matrix output selection circuitry.

Therefore those of ordinary skill within the art at the time of the invention would have been motivated to have the output selection circuit configured to output such outputs within the different cycles of the test mode within Deb wherein a tester or circuitry/device/unit receiving the output signals is configured to identify the outputs in such a way, such that a proper result can be accredited to the proper corresponding test and subsequent tested circuitry.

6. As per claim 11, Deb teaches the circuit/method as described above.

Deb does not specifically teacher the method where sending remaining output signals includes sending (i+1)th output signals (i being a positive integer) to ith data output pins.

However those of ordinary skill within the art at the time the invention was made would recognize that the method is not only limited to sending remaining output signals includes sending (i+1)th output signals (i being a positive integer) to ith data output pins during a second cycle/phase of the test mode. Those of ordinary skill in the art at the time the invention was made would recognize that any such configuration is well known when dealing with controllable switch-matrix output selection circuitry.

Therefore those of ordinary skill within the art at the time of the invention would have been motivated to have the method output such outputs within the different cycles/phases of the test mode within Deb wherein a tester or circuitry/device/unit receiving the output signals is configured to identify the outputs in such a way, such that

a proper result can be accredited to the proper corresponding test and subsequent tested circuitry

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Blumenau (U.S. Patent 5506510) discloses at least two different cycles of testing (column 2 lines 7-10) wherein a multiplexer unit is a switching matrix that responds to signals from a test controller to interconnect a DUT (device under test) to a tester or test circuitry wherein the number of pins between the two units is not identical and wherein the multiplexer switching matrix does not take up space within the IC (integrated circuit) which is increasingly becoming densely populated with electrical components.

ii. Godiwala et al (U.S. Patent 5712858) discloses a probe card figures 1-4 with different configurations to interconnect a conventional testing unit to a device under test (DUT) having a different amount of test pins/connections than the tester wherein the probe card may comprise switches that would allow interconnections between specific points at different time intervals thus indicating different cycles of testing communication between a conventional tester and a DUT.

iii. Mydill et al (U.S. Patent 5025205) discloses a switch matrix to interconnect an electronic pin output/input to any number of locations within a reconfigurable architecture for logic test.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100